

An EMC Design Risk Assessment Technique: To Retest or Not to Retest?

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Abstract: A technique is presented that provides for a qualitative and quantitative assessment of the risk of failing to achieve EMC compliance when making minor hardware design changes (component or PCB layout) on a product that has already had a successful compliance test performed. The EMC Design Risk Assessment (EDRA) technique uses a simple summation of risk scheme to allow design changes to be gauged and the requirement for re-testing to be implied from the total risk value. The technique allows a product supplier to make a quantified technical assessment of the impact of design changes on the compliance status and hence decide if a retest is required or can be avoided. The supplier may make the decision to not implement all of the suggested design changes in order to avoid retest costs and the EDRA may be used to determine which changes are not economically feasible.

Keywords: design risk assessment, technical construction file, qualitative assessment, re-test.

Introduction

Products are occasionally subject to minor modifications after EMC compliance testing has been performed. A complete retest may be overly expensive in relation to the required modification (maybe a resistor change or moving of a track on a PCB), hence the product supplier may decide not to retest. In many cases this will be acceptable as the change is unlikely to effect the EMC performance, but if a product did fail at a later date, could the company show due diligence in omitting to retest without evidence that they had considered the effect of the change?

Presented here is an EMC design risk assessment (EDRA) technique that provides both a qualitative and quantitative technique for assessing the impact of individual design changes on the compliance test status of a product. The technique is based on Design Failure Mode and Effect Analysis (DFMEA), a method used extensively in automotive and aerospace electronics and consequently should be familiar to many engineers. Having a basis in existing engineering practice should enable the technique to gain some credibility with DFMEA proponents and offer newcomers to the technique some level of confidence. It is presented here in a basic format for further development and expansion of the database of examples and risk values.

EMC Test Results

The results of successful EMC compliance tests are hopefully familiar to readers of this text; typically results consist of spectra of emissions with limit lines and simple "pass" for the immunity and ESD tests with their applied standards. The emission results can make assessing the effect of a change relatively easy (particularly if there is a lot of headroom between the result and the limit lines), but the lack of detail makes it difficult to assess the true impact on immunity and ESD performance; there is no quantitative information on how close to the pass limit the results are.

Impact and Risk Assessment

The use of existing knowledge of the effect of minor design changes, from the experiences of multiple projects and the collective experience of many different designs, allows a simple qualitative assessment of the risk of these changes and their relative effect on the EMC performance of any given design. There is an additional impact assessment that can be used to determine the likely measurable effect of the risk, based on the application of the change within EMC critical circuits (e.g. frequency dependent or input-output circuits). The risk factors can be modified to apply to specific industries (telecommunications, automotive, white goods etc.), but the impact assessment should be generic to all electronic modules and products and their EMC performance.

EMC Design Risk Assessment Technique

The EDRA technique is based on 4 categories of risk (implied effect), each category has numeric range to indicate level of EMC risk within the category (table 1).

Table 1: EDRA Risk Categories

Risk Categories	Value
None	0
Low	1 - 3
Medium	4 - 6
High	7 - 9

The impact assessment is a simpler multiplier based on the circuit application, low (1) for internal steady state only

circuits, medium (2) for any frequency dependant circuits that are not directly connected to input-output (I/O) circuits and high impact (3) for any I/O circuits (table 2). The risk factor is multiplied by the impact factor for each proposed circuit change.

Table 2: EDRA Impact Categories

Impact Categories	Value
Low	1
Medium	2
High	3

Consequently a simple change such as a change in a bias resistor value has in itself a low risk on system EMC performance. However, if this bias resistor is connected to an I/O circuit there is the potential that this will reduce the immunity of that circuit hence has a greater impact than if this is simply holding up an unused internal logic gate. It is also important to include changes that have no implied EMC risk, such as change in temperature performance, as this still demonstrates that the change was considered.

The category values are open to discussion and may be set for specific industries, values quoted here should be appropriate for an electronic module of moderate complexity (e.g. PC plug-in card or similar sized electronic controller). Highly complex, higher component density systems (e.g. PC's or instrumentation systems) may use slightly higher threshold values as higher component count systems may be less affected by single component changes.

Risk Categories;

Risk categories are based solely on the change proposed.

None: risk has no conceivable influence on the EMC or the proposed change has been tested in the circuit and proven to have no effect. An example is the use of a commercial temperature graded part rather than a military temperature part; EMC risk=0.

Low: minimal risk to EMC, other data is available to support the influence and suggests negligible impact. For example a pull-up or bias resistor value change from 5k Ω to 10k Ω ; EMC risk=1, increasing a power track length by a small amount (less than 10mm); EMC risk=2, moving an interface IC closer to a connector (could actually improve emissions but worsen ESD); EMC risk=3.

Medium: an increase in some aspects of EMC can be expected but not enough in any individual case to cause an increase of more than 3dB in emissions or effect immunity. Examples include reducing a bias resistor by more than 50% (i.e. reducing a 47k Ω to 4k7 Ω); EMC risk=4, changing a single de-coupling capacitor by approximately 50% of its current values (i.e. using a 470nF capacitor where a 1uF had been placed or vice versa); EMC risk=5, reducing the ground plane coverage by up to 25%; EMC risk=6.

High: major change is expected in EMC performance exceeding 3dB in emissions or reducing immunity/ESD protection. Examples include changing an interface IC (e.g. RS232 to RS422); EMC risk=7, changing a crystal clock (e.g. 20MHz to 32MHz); EMC risk=8 or changing a microprocessor (e.g. 8051 to PIC) or main power supply switcher IC; EMC risk=9.

The choice of risk level is somewhat subjective, but most experienced designers and compliance engineers should be able to make an educated assessment of the likely effect of individual changes within a circuit on the EMC performance of a product on this 10-point scale. Particularly as this assessment is provided after testing and hence information on the performance already achieved is available.

The assessment can be applied to the activity of embedded software as well as the physical electrical components. For example the software in many high-end microprocessors is responsible for the operating frequency of the system, the clock is often supplied by a lower frequency device and multiplied on-board by a factor set by the initialization code for system operation. Similarly the software may also determine interface data rates.

Impact Categories;

Impact categories are based solely on the application circuit to which the change is applied and the likelihood that these will be manifest outside of the system.

Low: impact is unlikely to be manifest outside of the product itself. Circuits affected are bias or steady state circuits and have no influence on the frequency content of the system or on the I/O; impact=1.

Medium: change will alter some frequency dependant content of the circuit or system, either filter circuit or oscillator circuit. Circuit does not directly interface with I/O but frequency change may be observed on supply line; impact=2.

High: circuits are directly connected to the I/O (including supply line), hence any change will be manifest to the external EM environment. Circuits may or may not affect frequency content; impact=3.

The effect of the impact category is to increase the relative risk value of those changes that are likely to directly affect measured EMC performance. Hence a change in de-coupling capacitor on an internal logic level will have a lower influence than a similar change on a serial data line IC connected to external circuits.

To Retest or Not to Retest

The sum of impact multiplied risk from the quantitative assessment, the result should provide three retest categories; none, partial, full. The basic premise is that no re-testing would be required if the EDRA sums to less than 30, some re-testing should be performed if the EDRA is between 30

and 60 and full re-test if the EDRA result exceeds 60. The partial re-test would typically be a single test or a few specific tests that would be determined by the designer or EMC test engineer (e.g. ESD retest or radiated and conducted emissions).

The risk assessment of changes must be cumulative between any testing to maintain the validity of the original results that the risks are being assessed against. This also prevents the false use of the EDRA technique by making a series of minor changes that individually do not suggest a retest but cumulatively exceed the suggested retest limit. However, after a full re-test the EDRA value is reset to zero for further design changes.

Design Examples

To illustrate the technique the following examples have been compiled.

Example A: Bench Top Instrument

A weighting machine using a 10MHz clocked microprocessor, 9600 baud RS232 interface, small LCD display, load sensor and a 5W, 50kHz switched mode power supply (SMPS). The manufacturer has a requirement for a similar instrument in the same metal housing, to measure a greater load (hence new load sensor) and with a 33400 baud, RS423 interface using the same microprocessor running at

16MHz.

The EDRA produces a risk value of 63 (table 3) suggesting a complete retest. The interface IC may have a similar ESD protection built-in so that this test could be omitted from retest, but immunity and emissions will be effected by the change in interface standard and microprocessor speed. What might have been perceived as a major change, the load sensor, is in fact minor in EMC terms as a similar output analogue strain gauge was used and the placement was identical within the instrument.

Example B: PC Plug-In Card

A PC plug-in card featuring 8MB video RAM, RGB digitizing input and output with on-board real-time processing of the video image. The unit is to be upgraded from 8-bit to 10-bit capture on the video with double on-board memory. The internal clock speed is increased from 100MHz to 125MHz on the DSP while maintaining the same base crystal frequency of 25MHz (the internal multiplier increases from 4 to 5 in the PLL register).

The EDRA produces a risk value of 33 (table 4) suggesting a partial retest. The interface components are likely to be of similar ESD tolerance, but the higher bit density of the new analogue-to-digital (A/D) converter is potentially more susceptible to noise at the video input. The change in operating frequency of the DSP will have minimal effect on

Table 3: Example A EDRA

Ref.	Problem	Risk	Risk Value	Impact	EDRA	
U17	Change serial interface	MED	6	3	18	
A11	Increase serial interface data rate >2x <5x	MED	6	3	18	
C3	Increase de-coupling capacitor by <50%	MED	4	3	12	
X6	Increase crystal frequency by more than 25%	HIGH	7	2	14	
X9	Change load sensor	LOW	1	1	1	
FULL RETEST					Total =	63

Table 4: Example B EDRA

Ref.	Problem	Risk	Risk Value	Impact	EDRA	
U15	Replace memory with higher density device	MED	5	1	5	
U20	Increase bit depth of ADC/DAC	MED	6	3	18	
X5	Increase crystal frequency by less than 25%	MED	5	2	10	
PARTIAL RETEST					Total =	33

Table 5: Example C EDRA

Ref.	Problem	Risk	Risk Value	Impact	EDRA	
R16	Add pull-up resistor to floating circuit	LOW	3	3	9	
C3	Increase de-coupling capacitor by <50%	MED	4	1	4	
Q3	Increase in breakdown voltage by more than 25%	LOW	1	3	3	
PCB5	Increase ground plane coverage	LOW	2	1	2	
NO RETEST					Total =	18

the radiated and conducted emissions since the base crystal is unchanged and edge rates will remain the same. The greatest effect will be in the repetition rate in the conducted band and the introduction of a 125MHz peak in the radiated emissions spectra replacing any 100MHz emission. Consequently partial retest might include radiated immunity, with particular attention to the video input, conducted emissions if the existing emission levels are close to the limit lines in the upper frequency range and radiated emissions testing again if the previous results were close to the limit lines.

Example C: Automotive Telematic Unit

A telematic unit currently has a high (battery) level input signal line, a new vehicle requirement has grounded switches only, hence a modification of the input circuit is required (the input will be tied to the battery supply on the PCB). Another output has a switch transistor that had been dropped by the supplier and replaced with a higher breakdown voltage version, the de-coupling capacitor for the microprocessor was increased and the ground plane was extended.

The EDRA produces a risk value of 18 (table 5) suggesting no re-testing is required due to these design changes. The main potential threat is reduced immunity from the pull-up resistor on the input as any battery transients will then be superimposed on the input when inactive, but overall the risk is still low.

Examples Database

An Excel spreadsheet of examples and proposed risk values is available to readers (via e-mail from the author). The spreadsheet provides the basis of an expanding knowledge base that can be contributed to by any reader and hence constructed from the experience of collective designs (without disclosing design details). The risk and impact categories should be appropriate to most categories of electronic designs and the main differences between applications could be the total risk level at which retest is suggested.

Another potential change would be to produce risk categories for each type of test (i.e. emission, immunity and ESD) but this would make the system more complicated to apply and therefore reduce its potential uptake and acceptance. There is also a corollary argument that the tests are linked and similar risk values would appear in all columns if the risk values were separated by test type.

Conclusion

The EMC design risk assessment (EDRA) technique proposed in this paper offers a simple low cost method of assessing the impact of design changes on the EMC performance of a circuit or product that has already been compliance tested. The method can be used to assess the effect of proposed changes or determine if the proposed

changes are economically viable in light of their requirement for an EMC retest.

The EDRA method can only be applied to products that do not require certified approval (i.e. self-certified products only). The EDRA results can be used within a Technical Construction File (TCF) with existing test data to prove that design changes that have not been re-tested have at least been technically assessed by the design authority.

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Biographical Notes



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